

TL592B DIFFERENTIAL VIDEO AMPLIFIER

SLFS001A – JUNE 1985 – REVISED APRIL 1988

- Adjustable Gain to 400 Typ
- No Frequency Compensation Required
- Low Noise . . . 3 μV Typ V_n

description

This device is a monolithic two-stage video amplifier with differential inputs and differential outputs. It features internal series-shunt feedback that provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

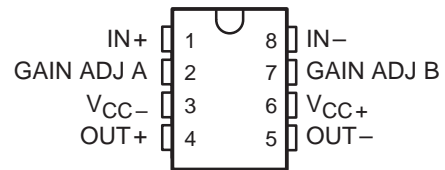
The differential gain is typically 400 when the gain adjust pins are connected together, or amplification may be adjusted for near 0 to 400 by the use of a single external resistor connected between the gain adjustment pins A and B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disk-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general-purpose video and pulse amplifiers.

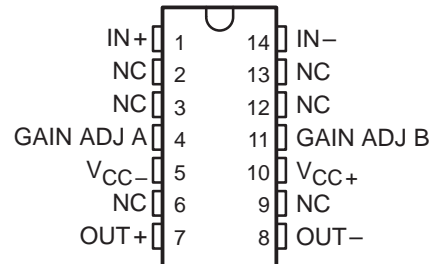
The device achieves low equivalent noise voltage through special processing and a new circuit layout incorporating input transistors with low base resistance.

The TL592B is characterized for operation from 0°C to 70°C.

D8† OR P PACKAGE
(TOP VIEW)

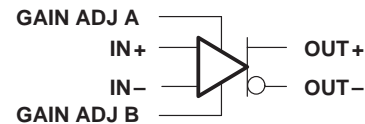


D14† OR N PACKAGE
(TOP VIEW)



† D8 and D14 are the codes to differentiate the 8-pin and 14-pin versions, respectively.

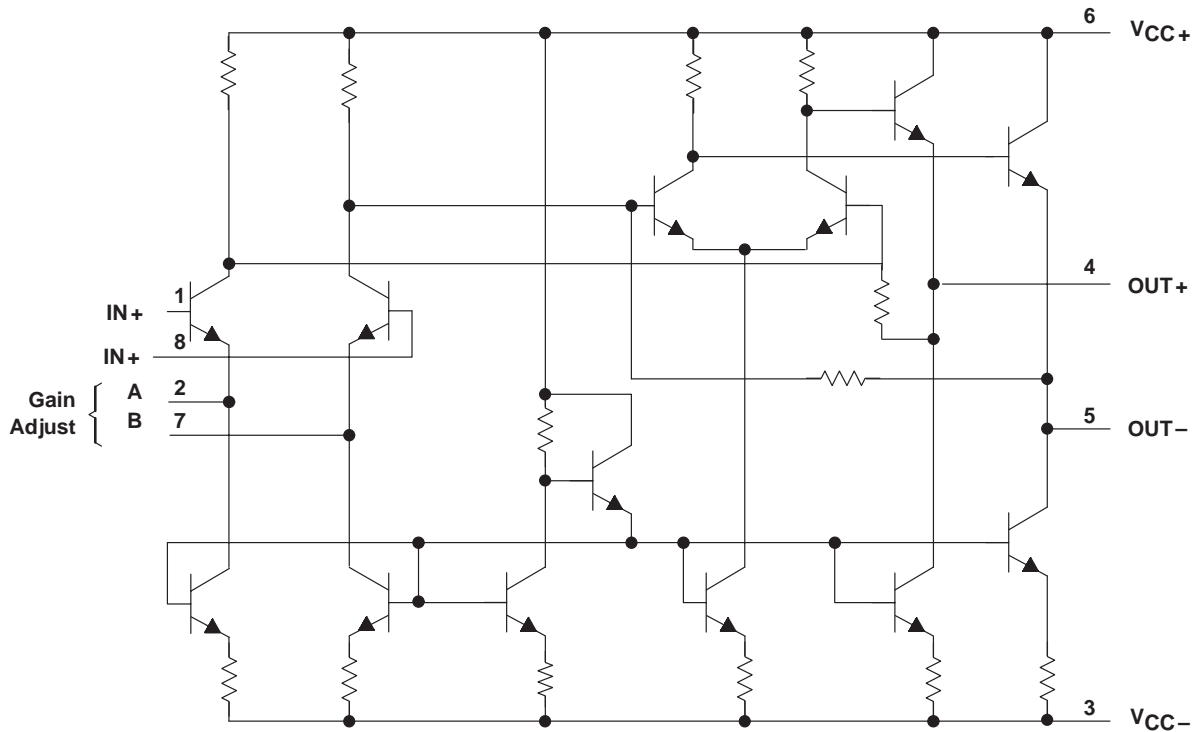
symbol



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schematic



Pin numbers are for D8 and P packages.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	8 V
Supply voltage, V_{CC-}	-8 V
Differential input voltage	± 5 V
Voltage range, any input	V_{CC+} to V_{CC-}
Output current	10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values except differential input voltages are with respect to the midpoint between V_{CC+} and V_{CC-} .

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70^\circ\text{C}$ POWER RATING
D8	530 mW	5.8 mW/°C	59°C	464 mW
D14	530 mW	N/A	N/A	530 mW
N	530 mW	N/A	N/A	530 mW
P	530 mW	N/A	N/A	530 mW

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	3	6	8	V
Supply voltage, V_{CC-}	-3	-6	-8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 6$ V, $R_L = 2$ k Ω (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITION [†]	T_A	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{OPP} = 3$ V, $R_L = 2$ k Ω , $R_{AB} = 0$	25°C	300	400	500	V/V
				0°C to 70°C	250		600	
A_{VD2}	Large-signal differential voltage amplification	1	$V_{OPP} = 3$ V, $R_L = 2$ k Ω , $R_{AB} = 1$ k Ω	25°C		13		V/V
BW	Bandwidth (-3 dB)	2	$V_{OPP} = 1$ V, $R_{AB} = 0$	25°C		50		MHz
I_{IO}	Input offset current			25°C		0.4	5	μ A
				0°C to 70°C			6	
I_{IB}	Input bias current			25°C		9	30	μ A
				0°C to 70°C			40	
V_{ICR}	Common-mode input voltage range	3		25°C	± 1			V
				0°C to 70°C	± 1			
V_{OC}	Common-mode output voltage	1	$R_L = \infty$	25°C	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1	$V_{ID} = 0$, $R_L = \infty$, $R_{AB} = \infty$	25°C		0.35	0.75	V
				0°C to 70°C			1.5	
V_{OPP}	Peak-to-peak output voltage swing	1	$R_L = 2$ k Ω , $R_{AB} = 0$	25°C	3	4		V
				0°C to 70°C	2.8			
r_i	Input resistance		$V_{OD} = 1$ V, $R_{AB} = 0$	25°C		4		k Ω
				0°C to 70°C		3.6		
r_o	Output resistance			0°C to 70°C			30	Ω
C_i	Input capacitance			25°C		5		pF
$CMRR$	Common-mode rejection ratio	3	$V_{IC} = \pm 1$ V, $R_{AB} = 0$	f = 100 kHz	25°C	60	86	dB
				f = 5 MHz		60		
				f = 100 kHz	0°C to 70°C	50		
				f = 5 MHz		60		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC+}/\Delta V_{IO}$)	4	$\Delta V_{CC+} = \pm 0.5$ V, $\Delta V_{CC-} = \pm 0.5$ V, $R_{AB} = 0$	25°C	50	70		dB
				0°C to 70°C	50			
V_n	Broadband equivalent input noise voltage	4	BW = 1 kHz to 10 MHz	25°C		3		μ V
t_{pd}	Propagation delay time	2	$\Delta V_O = 1$ V	25°C		7.5		ns
t_r	Rise time	2	$\Delta V_O = 1$ V	25°C		10.5		ns
$I_{sink(max)}$	Maximum output sink current		$V_{ID} = 1$ V, $V_O = 3$ V		3	4		mA
I_{CC}	Supply current		No load, No signal	25°C		18	24	mA
				0°C to 70°C			27	

[†] R_{AB} is the gain-adjustment resistor connected between gain-adjust pins A and B. If not specified for a particular parameter, its value is irrelevant to that parameter.



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PARAMETER MEASUREMENT INFORMATION

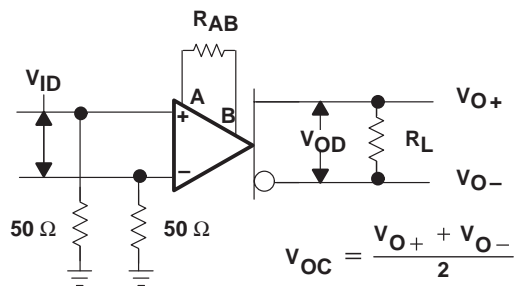


Figure 1

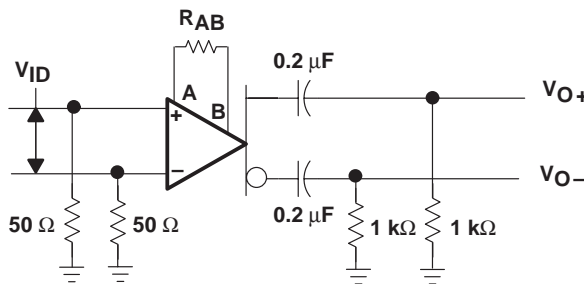


Figure 2

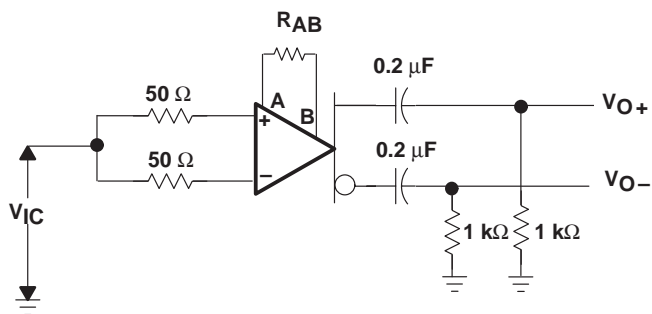


Figure 3

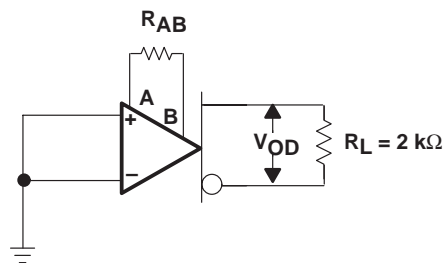


Figure 4

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

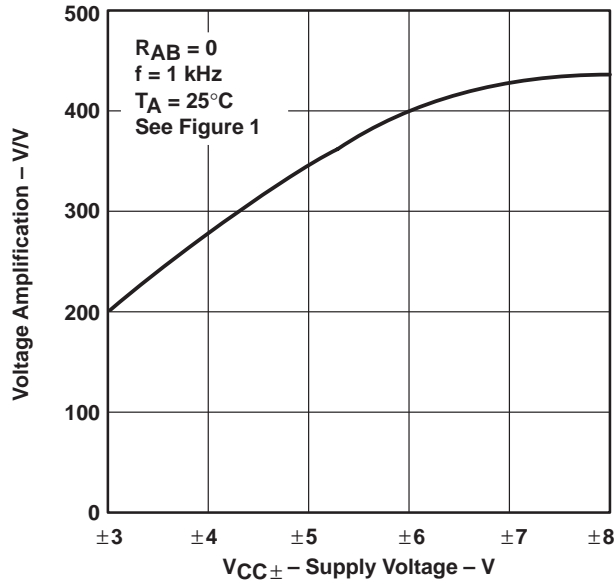


Figure 5

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
GAIN-ADJUSTMENT RESISTANCE

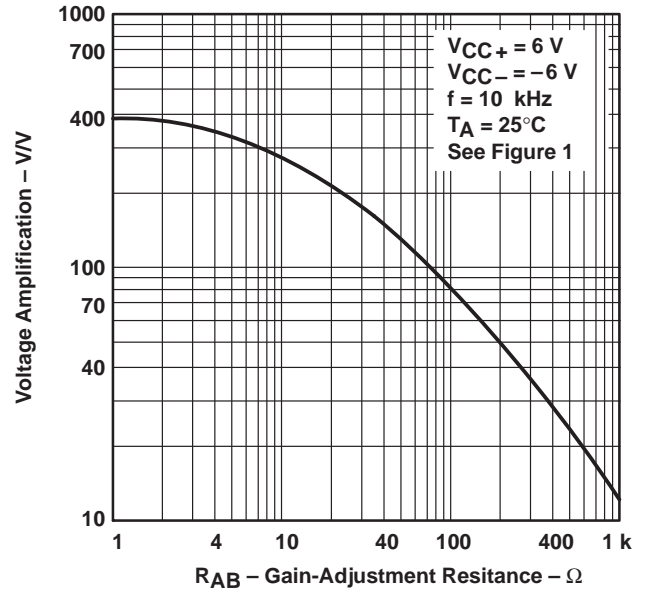


Figure 6

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

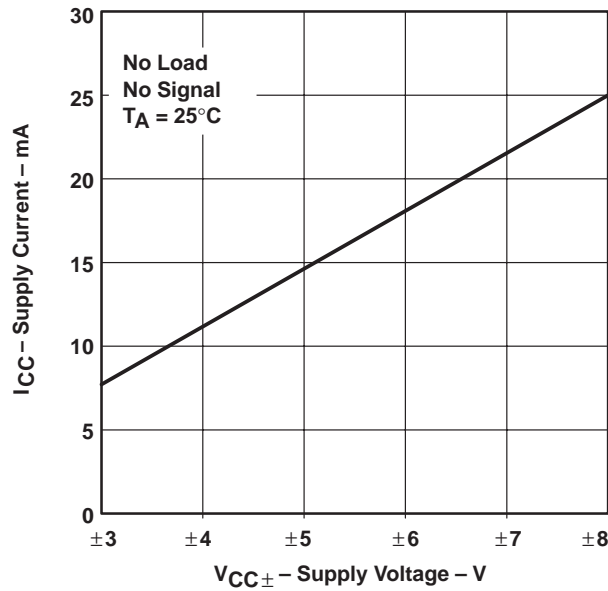


Figure 7

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TL592B-8D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL592B-8DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL592B-8DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL592B-8DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL592BI-8D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL592BN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
TL592BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL592BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL592BPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL592BPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

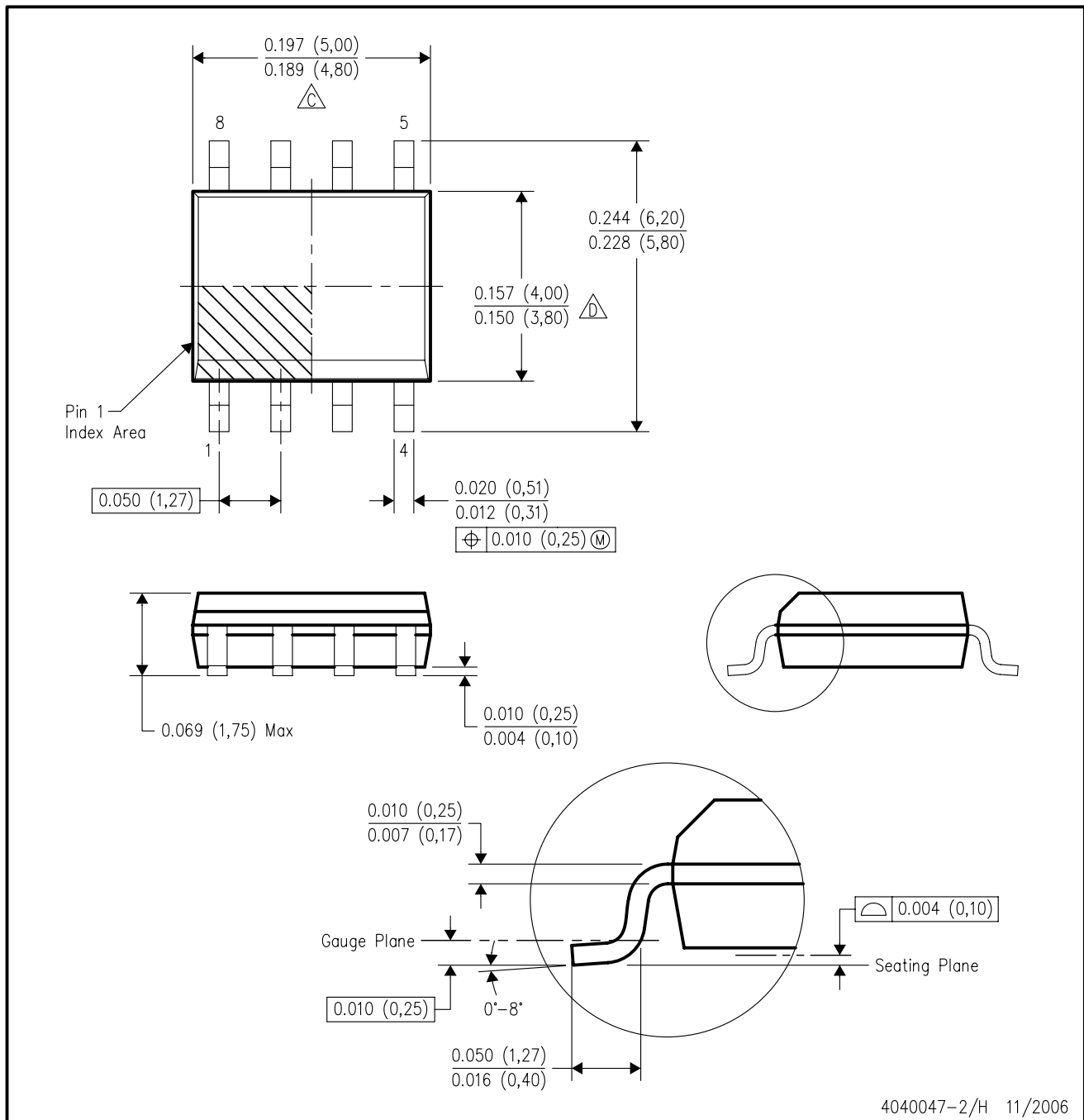
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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